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1. Cache design for eliminating the address translation bottleneck and reducing the tag area
 Yen-Jen Chang, Feipei Lai, Shang-Jang Ruan.
Computer Design, VLSI in Computers and Processors, 2002. Proceedings. 2002 IEEE International 16-18 Sept. 2002 Page(s) 334 - 339
 Digital Object Identifier 10.1109/ICCD.2002.1106791
[AbstractPlus](#) | [Full Text: PDF\(1339 KB\)](#) [IEEE CNF](#)
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2. Direct addressed caches for reduced power consumption
 Witchel, E.; Larsen, S.; Ananian, C.S.; Asanovic, K.;
Microarchitecture, 2001. MICRO-34. Proceedings. 34th ACM/IEEE International Symposium on 1-5 Dec. 2001 Page(s) 124 - 133
 Digital Object Identifier 10.1109/MICRO.2001.991111
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[Rights and Permissions](#)
3. SAME-LSQ: set-associative multiple-instruction entry load/store queue
 Abella, J.; Gonzalez, A.;
Parallel and Distributed Processing Symposium, 2006. IPDPS 2006. 20th International 25-29 April 2006 Page(s) 10 pp.
 Digital Object Identifier 10.1109/IPDPS.2006.1639290
[AbstractPlus](#) | [Full Text: PDF\(192 KB\)](#) [IEEE CNF](#)
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4. Piezoelectric transformer for integrated MOSFET and IGBT gate driver
 Vasic, D.; Costa, F.; Sarraute, E.;
Power Electronics, IEEE Transactions on Volume 21, Issue 1, Jan. 2006 Page(s) 56 - 65
 Digital Object Identifier 10.1109/TPEL.2005.861121
[AbstractPlus](#) | [Full Text: PDF\(1160 KB\)](#) [IEEE JNL](#)
[Rights and Permissions](#)
5. Improving performance of large physically indexed caches by decoupling memory address
 Rui Min, Yiming Hu,

Computers, IEEE Transactions on

Volume 50, Issue 11, Nov. 2001 Page(s):1191 - 1201

Digital Object Identifier 10.1109/12.966494

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Knaup, M.; Steckmann, S.; Bockenbach, O.; Kachelrieß, M.;

Nuclear Science Symposium Conference Record, 2007. NSS 07. IEEE

Volume 4, Oct. 26 2007-Nov. 3 2007 Page(s):3074 - 3076

Digital Object Identifier 10.1109/NSSMIC.2007.4436779

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deLormier, M.; Kapre, N.; Mehta, N.; Rizzo, D.; Eslick, I.; Rubin, R.; Uribe, T.E.; Knight, T.F.; Del-

Field-Programmable Custom Computing Machines, 2006. FCCM '06. 14th Annual IEEE Symposium

April 2006 Page(s):143 - 151

Digital Object Identifier 10.1109/FCCM.2006.45

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Chang, D.C.-W.; Saxena, N.R.;

Fault-Tolerant Computing, 1993. FTCS-23. Digest of Papers., The Twenty-Third International Syn-

22-24 June 1993 Page(s):630 - 635

Digital Object Identifier 10.1109/FTCS.1993.627366

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